Modul Description

Module name	Course Module
Module level, if applicable	Bachelor of Electronics Engineering
Code, if applicable	5215-1822
Subtitle, if applicable	-
Course, if applicable	Logic Circuit
Semester(s) in which the module istaught	II
Person responsible for the module	Lecturer of Courses
Lecturer	Drs. Jusuf Bintoro, MT
Language	Indonesian Language [Bahasa Indonesia]
Relation to Curriculum	This course is a compulsory course and offered in the 2th semester.
Type of teaching, contact hours	Teaching methods used in this course are: - Lecture (i.e., group investigation, small group discussion, case study, and video-based learning) - Structured assignments (i.e., essays and case study) - Practice (i.e., computer simulation and case study in laboratorium) The class size for lecture is 30 students. Contact hours for lecture is 27 hours, assignments are 32 hours
Workload	For this course, students required to meet a minimum of 91 hours in one semester, which consist of: - 27 hours for lecture, - 32 hours for structured assignments, - 32 hours for private study,
Credit points	2 credit points (equivalent with 2.88 ECTS)
Requirements according to the examination regulations	Students must have attended all classes and submitted all class assignments that are scheduled before the final tests.
Recommended prerequisites	Students must have attended all classes and submitted all class assignments that are scheduled before the final tests.

PLO-CLO-ILO	After completing the course and given with this case: **Course Learning Objectives (CLO1):** Mahasiswa mampu memahami teori tentang Sistem Bilangan, Sistem Konversi antar Bilangan Dasar, Operasi Sistem Bilangan, Gerbang Logika, Aljabar Boolean, Karnough Map dan Kombinasi Rangkaian Logika. (K1) (10) **Course Learning Objectives (CLO2):** Mahasiswa mampu merancang sistem menggunakan gerbang logika (K2, S1, S3, C1) (25) **Course Learning Objectives (CLO3):** Mahasiswa mampu menerapkan Karnough Map pada Rangkaian Logika dan penggunaan Rangkaian Logika Sekuensial (K2, S1, S3, C1) (25) **Course Learning Objectives (CLO4):** Mahasiswa mampu melakukan pengujian rangkaian logika sederhana menggunakan software aplikasi logika (K2, S1, S3, C1) (40) **Program Learning Outcomes (PLO3):** Menerapkan kompetensi teknik elektronika untuk memecahkan masalah keteknikan **Knowledge (K1):** Menerapkan matematika, ilmu dasar dan teknik dasar untuk merancang dan menganalisis untuk memecahkan masalah di bidang teknik elektronika. **Knowledge (K2):** Untuk menerapkan prinsip-prinsip teknik elektronik untuk memecahkan masalah dalam sistem teknik elektronik **Engineering and Education Skill (S1):** Mampu merancang prinsip dan aplikasi sistem rekayasa elektronik **Engineering and Education Skill (S2):** Mampu menganalisis prinsip kerja dan penerapan sistem rekayasa elektronik **Engineering and Education Skill (S3):** Mampu mencari alternatif solusi dan pemecahan masalah di bidang teknik elektronika. **Competence (C1):** Menerapkan teknologi baru di bidang rekayasa dengan mempertimbangkan standar teknis, aspek kinerja, keandalan, penerapan, dan keberlanjutan

	Competence (C2): Mampu mengelola dan mengembangkan proses, sistem operasi, dan peralatan dengan mempertimbangkan dampak teknis dan nonteknis dari kegiatan industri di bidang teknik elektronika.
Content	**Students will learn about:** Mata Kuliah Rangkaian Logika merupakan kuliah teori tentang Sistem Bilangan, Sistem Konversi antar Bilangan Dasar, Operasi Sistem Bilangan, Gerbang Logika, Aljabar Boolean dan Karnough Map, Kombinasi Rangkaian Logika, Dasar Perancangan Sistem menggunakan gerbang logika dan pengujian rangkaian logika sederhana menggunakan software aplikasi logika.
Forms of Assessment	Assessment is carried out based on written examinations, assessment/evaluation of the learning process and performance with the following components: Attitude: 5%; General Skills: 5%; Special skill: 20%; Mid Test: 30%; Final Test: 40%
Study and examination requirements and forms of examination	**Study and examination requirements:** - Students must attend 15 minutes before the class starts. - Students must switch off all electronic devices. - Students must inform the lecturer if they will not attend the class due to sickness, etc. - Students must submit all class assignments before the deadline. - Students must attend the exam to get final grade. **Form of examination:** Written exam: Essay
Media employed	Direct Whiteboard and Power Point Presentation.
Reading list	Referensi Utama: 1. Ndjoutche, Tertulien. (2016). Electronics Engineering Series: Digital Electronics 1, Combinational Logics Circuits.Great Britain and the United States: ISTE Ltd and John Wiley & Sons, Inc. 2. Ndjoutche, Tertulien. (2016). Electronics Engineering Series: Digital Electronics 2 Sequential and Aritmetic Logic Circuit. Great Britain and the United States: ISTE Ltd and John Wiley & Sons, Inc 3. Sarkar, Subir Kumar, et.al. (2014). Foundation of Digital Electronics and Logic Design. Broken Sound Parkway NW, Suite 300: CRC PressTaylor & Francis Group Referensi Pendukung: 4. Nahin, Paul J. (2013). The Logician and the Engineer. New Jersey 08540: Princetown University Press. 5. Ndjoutche, Tertulien. (2016). Electronics Engineering Series: Digital Electronics 3 Sequential and Aritmetic Logic Circuit.

	Great Britain and the United States: ISTE Ltd and John Wiley & Sons, Inc 6. Referensi Pendukung lainnya yang dapat dibaca tidak terbatas pada nama pengarang; melalui internet browser (google, etc) dan youtube dengan kata kunci (Keyword): Rangkaian Logika atau Logic Circuit